I claim:

1. A buffer device, comprising:

an input line device for receiving input data;

a plurality of latch stages connected to said input line device, each of said latch stages including at least a latch device, a multiplexer, and a data output terminal;

said multiplexer having at least a first selection state and a second selection state, and said multiplexer being provided and configured in a respective one of said latch stages and being controllable such that said data output terminal is selectively supplied directly with the input data present at said input line device, when said multiplexer is in the first selection state, and said data output terminal is supplied with data buffered in said latch device, when said multiplexer is in the second selection state, for providing data with one of a selectable latency and a selectable delay;

an output line device for outputting output data corresponding to the input data;

said latch device of a first one of said latch stages, as seen from said output line device, having a feedback loop for data buffering; and

said multiplexer of said first one of said latch stages being associated with said feedback loop and being configured such that the output data on said output line device can be kept stable.

2. The buffer device according to claim 1, wherein said multiplexer of said first one of said latch stages is configured such that the output data on said output line device can be kept stable irrespective of an activation state of said latch device in said latch stages.

3. The buffer device according to claim 1, wherein said multiplexer of said first one of said latch stages is configured such that the output data on said output line device can be kept stable irrespective of a current change in the input data.

4. The buffer device according to claim 1, wherein each of said latch stages has at least one data input terminal.

5. The buffer device according to claim 4, wherein said latch stages are provided substantially in series such that, from said input line device to said output line device, said data output terminal of a respective preceding one of said latch

stages is connected to said at least one data input terminal of a directly following one of said latch stages.

6. The buffer device according to claim 1, wherein all of said latch stages have a substantially identical configuration.

7. The buffer device according to claim 1, wherein all of said latch stages operate in substantially a same manner.

8. The buffer device according to claim 1, wherein said multiplexer in each of said latch stages has a substantially identical configuration .

9. The buffer device according to claim 1, wherein said multiplexer is configured to receive a selection signal, said multiplexer is selectively brought into at least the first selection state and the second selection state with the selection signal.

10. The buffer device according to claim 9, wherein said multiplexer receives the selection signal in order to select one of a latency and a delay time.

11. The buffer device according to claim 1, wherein said latch device of said latch stages is in each case configured to receive a read signal for activating said latch device.

12. The buffer device according to claim 11, wherein said latch device is activated with the read signal in order to output data buffered in said latch device to said data output terminal of a respective one of said latch stages.

13. The buffer device according to claim 1, wherein at least one element selected from the group consisting of said latch device and said multiplexer of a respective one of said latch stages is configured to receive a clock signal for controlling a processing.

14. The buffer device according to claim 1, including a line device in each of said latch stages for feeding at least one signal selected from the group consisting of an input data signal, an activation signal, a selection signal and a clock signal.

15. The buffer device according to claim 1, wherein said line device is provided in said latch device of each of said latch stages.

16. The buffer device according to claim 1, wherein said latch device is a flipflop device.

17. The buffer device according to claim 1, wherein said latch device is a D-flipflop.

18. The buffer device according to claim 1, wherein said latch stages are configured such that at least one of a given sequence of said latch device of said latch stages and a selection signal defines selection possibilities for one of latencies and delay times.

19. The buffer device according to claim 16, wherein said latch stages are configured such that at least one of a given sequence of said flipflop device of said latch stages and a selection signal defines selection possibilities for one of latencies and delay times.

20. The buffer device according to claim 1, wherein said multiplexer of at most one of said latch stages is configured such that selection signals can bring said multiplexer into the second selection state.